REMARKS

Claims 1-6, 8-13, 15-20, and 22-24 are pending in the present application. Claims 7, 14, and 21 are canceled; claims 1, 4, 5, 8, 11, 12, 15, and 18-20 are amended; and claims 22-24 are added. Reconsideration of the claims is respectfully requested.

Amendments to claims 4, 5, 11, 12, and 18-20 correct typographical errors that do not change the scope of those claims. Support for the amendments to claims 1, 8, and 15 can be found in originally presented claims 7, 14, and 21. Support for new claims 22-24 can be found in Figure 5 and in the specification at page 22, first full paragraph through the second full paragraph. No new matter is added.

I. Interview Summary

On January 9, 2005, examiner Gu and the undersigned attorney discussed the rejections under 35 U.S.C. § 112, second paragraph. No agreement was reached.

II. Claim Objections

The examiner objects to claims 4, 11, and 18-21. Claim 21 has been canceled, thereby rendering the objection with respect to that claim moot. Claims 4, 11, and 18-20 have been amended accordingly, thereby overcoming the objections.

III. 35 U.S.C. § 112, Second Paragraph

The examiner rejects claims 7, 14, and 21 as indefinite. These claims have been canceled, thereby rendering the rejection moot.

IV. 35 U.S.C. § 102, Asserted Anticipation

The examiner rejects claims 1-6, 8-13 and 15-20 as anticipated by *Porter* et al., Computer System Operation with Corrected Read Data Function, U.S. Patent 5,263,032 (November 16, 1993) (hereinafter "*Porter*"). This rejection is respectfully traversed.

As to claims 1-6, 8-13 and 15-20, the Office Action states:

> As for claims 1, 8 and 15, Porter et al. discloses a method of managing memory in a computing device, comprising:
>
> receiving a notification (Co. 10, Lines 12-15; Col 14, Lines 63-65; Col 15 Lines 10-18) of a runtime correctable error associated (Fig 6, 66 and 69; Col 4 Lines 24-25; Col 5, Lines 13-14; Col 5, Lines 67-68; Col 6, Lines 1-5) with a memory cell (Col 5, Lines 64-66);
>
> determining if the runtime correctable error has persisted for longer than one memory scrub cycle (Col 5, Lines 41-68; Col 6, Lines 1-5); and
>
> requesting dynamic memory page deallocation for a page of memory associated with the memory cell with which the runtime correctable error is associated if the runtime correctable error has persisted for longer than one memory scrub cycle (Col 5, Lines 67-68; Col 6, Lines 1-17).
>
> The method of claim 1 is clearly performed by Porter et al.'s apparatus (Fig 1; Fig 2; Fig 3), and its computer program product and instructions (Col 15, Lines 10-61; Fig 6; Fig 7; Fig 8).

Office Action of February 29, 2005, pp. 2-3.

A prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). All limitations of the claimed invention must be considered when determining patentability. *In re Lowry*, 32 F.3d 1579, 1582, 32 U.S.P.Q.2d 1031, 1034 (Fed. Cir. 1994). Anticipation focuses on whether a claim reads on the product or process a prior art reference discloses, not on what the reference broadly teaches. *Kalman v. Kimberly-Clark Corp.*, 713 F.2d 760, 218 U.S.P.Q. 781 (Fed. Cir. 1983). In this case each and every feature of the presently claimed invention is not identically shown in the cited reference, arranged as they are in the claims.

Claim 1 as amended is as follows:

> 1. A method of managing memory in a computing device, comprising:
>
> receiving a notification of a runtime correctable error associated with a memory cell, wherein the receiving a notification step further comprises:
>
> determining if any memory extents in the memory have not been memory scrubbed;
>
> if memory extents exist that have not been memory scrubbed, identifying a next memory extent that has not been memory scrubbed;

scrubbing the next memory extent to identify any memory cell errors;

determining if any redundant bit lines are available for redundant bit line steering; and

receiving the notification of the runtime correctable error if redundant bit lines are available for redundant bit line steering;

determining if the runtime correctable error has persisted for longer than one memory scrub cycle; and

requesting dynamic memory page deallocation for a page of memory associated with the memory cell with which the runtime correctable error is associated if the runtime correctable error has persisted for longer than one memory scrub cycle.

Claim 1 as amended contains most of the features originally present in claim 7. As indicated by the specification at page 6, last paragraph, until the present invention redundant bit steering and dynamic memory page deallocation were considered mutually exclusive and not known in the prior art. Thus, combining these features in the manner presented in claim 1 is novel. Certainly, as apparently indicated by the examiner, *Porter* does not teach all of these features. Therefore, claim 1 should now be in condition for allowance.

In particular, *Porter* does not teach the features of determining if any redundant bit lines are available and receiving the notification if redundant bit lines are available for redundant bit line steering, at least in the context of the additional feature of requesting dynamic memory page deallocation for a page of memory associated with the memory cell. *Porter* does teach marking memory pages as "bad." For example, *Porter* teaches that:

> (4) When another correctable read error event occurs, the error is corrected and data sent back to CPU, and a footprint is generated as before. The footprint is compared to previous footprints and if a match occurs (and this location has already been scrubbed) the location is deemed to be a hard correctable error rather than a transient error, and so the page of memory 12 is replaced. Replacing the page entails assigning a new page frame number in the page table 17 for this page of virtual memory so it will be mapped to a different page (map 18) of physical memory 12. The data in the present page is read (and corrected), then rewritten to the new page frame. The old page frame number is marked "bad" and not used, as the page table is updated. The act of reading the page to copy it back to the new page frame will generate another correctable error, and thus would tend to produce an new footprint, but the new footprint is suppressed by noting that a page replacement is in process.

Porter, col. 5, l. 67 through col. 6, l. 17.

However, *Porter* does not teach bit line steering and *Porter* does not teach coordinating bit line steering with memory page deallocation. Nothing in the above text or elsewhere within *Porter* teaches or suggests either of these features. Therefore, *Porter* does not anticipate claim 1 as amended.

Claims 8 as amended and 15 as amended contain features similar to those presented in claim 1 as amended. Thus, *Porter* does not anticipate claims 8 and 15 at least for the reasons presented vis-à-vis claim 1. Furthermore, because claims 2-6, 9-13, 16-19, and 22-24 depend from claims 1, 8, or 15, *Porter* does not anticipate these claims at least for the reasons presented vis-à-vis claim 1. Additionally, claims 2-6, 9-13, 16-19, and 22-24 claim other additional combinations of features not suggested by the reference. For example, claims 22-24 contain features directed to determining if a predetermined threshold number of memory cell errors is exceeded during the scrubbing of the memory and, if the predetermined threshold number of memory cell errors is exceeded, performing redundant bit line steering. *Porter* does not teach or suggest these features. Consequently, it is respectfully urged that the rejection of claims 1-6, 8-13, 15-19, and 22-24 have been overcome.

Furthermore, *Porter* does not teach, suggest, or give any incentive to make the needed changes to reach the presently claimed invention. Absent the examiner pointing out some teaching or incentive to implement combining memory page deallocation and bit line steering in view of *Porter*, one of ordinary skill in the art would not be led to modify *Porter* to reach the present invention when the reference is examined as a whole. Absent some teaching, suggestion, or incentive to modify *Porter* in this manner, the presently claimed invention can be reached only through an improper use of hindsight using Applicants' disclosure as a template to make the necessary changes to reach the claimed invention.

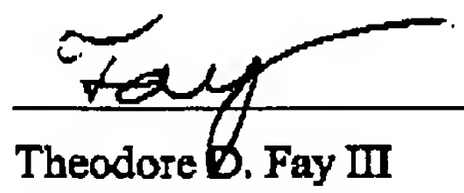
V. Conclusion

It is respectfully urged that the subject application is patentable over *Porter* and is now in condition for allowance.

The examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

DATE: January 11, 2006

Respectfully submitted,



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